ABSTRACT OF THE DISCLOSURE

First buffers of a first driver circuit generate voltages to be supplied to word lines, respectively. Second buffers of a second driver circuit operate in synchronization with the first buffers to generate voltages to be supplied to first substrate lines, respectively. Each second buffer, upon access to memory cells, supplies a voltage for lowering the threshold values of transfer transistors and driver transistors to its corresponding first substrate line, and supplies thereto a voltage for raising the threshold values of the transfer transistors and the driver transistors during standby. This can improve the operation speed at the time of accessing the memory cells and reduce the leak current during standby. This results in shortening the access time during the operation of the semiconductor memory and reducing the standby current during standby.